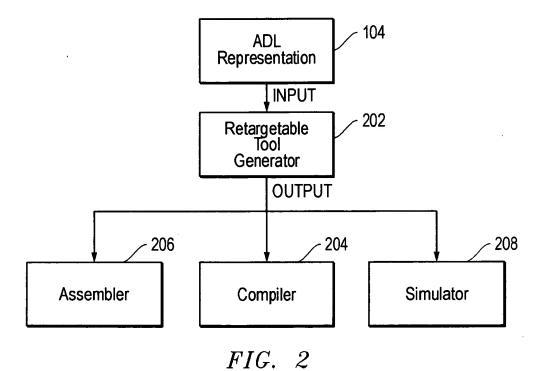


FIG. 1





| Arm Instruction Bet Opnd Order Description 702 Data pino inm cond. C 710 CP_num -712 opcode 1 CDP opcode_1 714 CRn CRm opcode_2 12 bit offset 8-bit offset 8_bit_immediat rotata_mmed RdLo 716 -704 Data proc intr MOVS MVNS ADDS Data Processin Rm Shift shift_Immed register list register_list_15 24 bit immedia 0 0 0 1 1 0 0 S Rn
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0 0 T S Rn
0 0 T S Rn
0 T cond nsis chitt Rm cond TEOS Hm. Am 0 0 0 0 shift immed shift Oata proc. ned Data proc. register_shift MOVR cond CORE Am Am Am R9 Rs MVNP 00014 Rs cond Hm Rm Hm ADCA Rd HS HS O shilt 1 cond SURF cond SBCP 0 sh 0 sh 0 sh 0 sh 盟 COL Am Am RSBF ASOF 罪 Hd COD ANDR EORR ORRR Rm Am Rd As 000 Rm Rm Rm HS His BICA CMPA CMNA cond 0 0 0 0 0 0 0 0 0 0 0 0 cond CORE **Juliply** Mortiply
Multiply Accumulate
Multiply Long
Signed Multiply Accumulate Long
Signed Multiply Accumulate Long
Unsigned Multiply Accumulate Long
Unsigned Multiply Long
Unsigned Multiply Long cond 6n 0 0 0 0 CORC Rd o cond Multiply Long cond PdLo SMULL PdLo cond UMLAL RdLo cond Move from Status regidter Move immediate to Status regidte cond · Rd conc 1 1 1 1 ctate_mmed 8 bt_m cond Move register to Status regidier Brach Instructio Rd MSA cond 欧山 Brach and exchi Am COTA Load/Store imm Load/Store imi LDRI cond Rη DABI cond LDAB'TI LDATI cond Hd Ad 12 bit offset cond STRI STRBI STRBT Ad 12 bit ollset cond 12 bit allsed മാവ 띪

FIG. 7



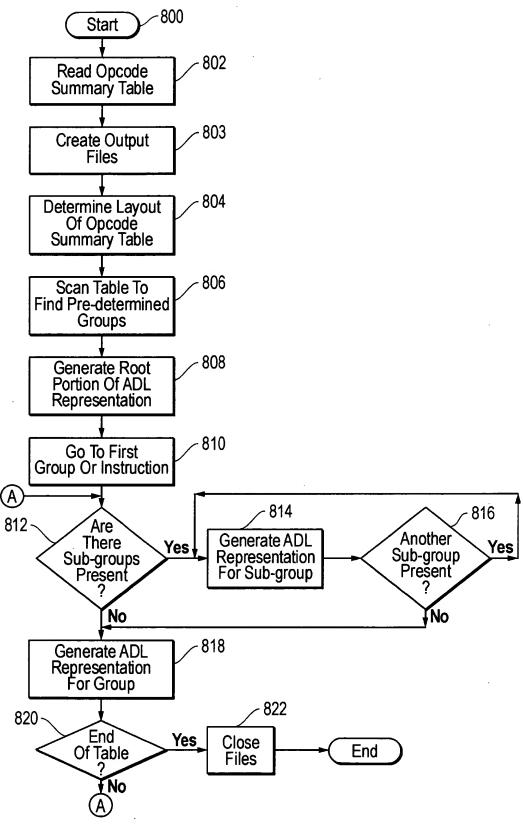


FIG. 8